REMARKS

Claims 1-3, 5, 7-8 and 10 are currently amended and claims 12-15 are added. Claims 1-15 are now pending. Applicant contends that the amendments contained herein and the added claims are supported by the Specification as filed and thus do not constitute new matter.

In the Drawings

Figure 33 was amended to correct a typographical error in the formal drawings. Applicant has submitted a Red-lined Figure 33 and Thirty-six (36) sheets of replacement formal drawings for the Examiner's review.

Claim Rejections Under 35 U.S.C. § 112

Claim 7 was rejected under 35 U.S.C. §112, first paragraph, as failing to comply with enablement requirement. Claim 7, as currently amended, recites in part, "wherein the plurality of addressable banks comprise four banks." Applicant maintains that the limiting of a plurality of addressable banks to four addressable banks is supported by the specification. Applicant respectfully requests reconsideration and withdrawal of the rejection, and allowance of claim 7.

Claim Rejections Under 35 U.S.C. § 103

Claims 1-6 and 8-11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Schumann et al. (U.S. Patent No. 5,732,017) in view of Lee (U.S. Patent No. 5,307,314). Claims 1-6 and 8-11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Pashley et al. (U.S. Patent No. 6,418,506) in view of Lee (U.S. Patent No. 5,307,314). Claims 1-6 and 8-11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Akaogi et al. (U.S. Patent No. 6,240,040) in view of Lee (U.S. Patent No. 5,307,314). Applicant respectfully traverses these rejections.

Each of claims 1 and 5, as currently amended, includes read/write circuitry that writes first data provided by a first processor to a first one of a plurality of addressable banks of a single array of non-volatile memory cells and simultaneously reads two or more second data from a second one of the plurality of addressable banks and provides the two or more second data to a

second processor. Each of claims 2 and 10, as currently amended, includes receiving first data from a first external processor coupled to the memory, writing the first data to a first location in a memory array of the non-volatile memory device, substantially simultaneously reading two or more second data from a second location in the memory array of the non-volatile memory device, and outputting the two or more second data to a second external processor coupled to the memory device.

Applicant carefully reviewed Schumann et al., Pashley et al., and Akaogi et al. and found no indication of read/write circuitry that writes first data to a first one of a plurality of addressable banks of an array of non-volatile memory cells and simultaneously reads two or more second data from a remaining bank of the plurality of addressable banks of the array of non-volatile memory cells, as in each of claims 1 and 5. This means that each of claims 1 and 5 writes to and simultaneously reads from the *same* array of non-volatile memory cells.

In contrast, Schumann et al. concurrently reads flash memory 11 during a write cycle period of a *separate* E^{2}PROM array 13 (Figure 1 and column 6, lines 43-44). In Schumann et al., an E^{2}PROM read cannot be performed during any of the write cycles (column 7, lines 27-28). Pashley et al. reads from a RAM array during at least a portion of a period of time in which data is written to a *separate* flash array (column 5, lines 11-14). Alternatively, Pashley et al. writes to the RAM array during at least a portion of a period of time in which data is read from the *separate* flash array (column 5, lines 14-18).

In each of claims 1 and 5, read/write circuitry writes first data to a first one of the plurality of addressable banks and simultaneously reads *two or more second data* from a second remaining bank of the plurality of addressable banks. However, in Akaogi et al., for the duration of a read operation at one bank of N banks, a *single* write operation can *only* be performed on any *one* of the other N-1 banks, and for the duration of a write operation at one bank of the N banks, a *single* read operation can *only* be performed on any one of the other N-1 banks (column 2, lines 56-60).

In Lee, a volatile memory (DRAM) allows for simultaneous read and write operations which are performed across the same addressed row of two or more banks, and for the duration of the simultaneous read and write operations *only one* operation can occur on the same addressed row on *each* bank (column 4, lines 20-29, column 5, line 65 to column 6, line 1, column 12, lines 3-29). Lee also requires that the data I/O be split into two or more parts for

these split read/write operations such that different I/O ports read data and/or write data during the same communication exchange and does not copy the write data into a write latch (column 4, lines 47-63, column 9, lines 4-25). Applicant respectfully submits that, because of the split data I/O, the requirement that the same row be accessed across all banks, and a single read and/or write operation occurring on each bank during the duration of the simultaneous access, Lee does not teach independent access of the memory by two processors. Applicant also notes that the timing of read and write cycles of a non-volatile memory array differ and are non-analogous to that of a volatile memory array, where they are substantially similar in duration.

In view of the above, Applicant respectfully submits that neither Schumann et al., Pashley et al., nor Akaogi et al. either alone or in combination with Lee teach or suggest each and every element of each of independent claims 1 and 5. Therefore, each of claims 1 and 5 should be allowed.

Claims 2 and 10 include receiving first data from a first external processor coupled to the memory, writing the first data to a first location in a memory array of the non-volatile memory device, substantially simultaneously reading two or more second data from a second location in the memory array of the non-volatile memory device, and outputting the second data to a second external processor coupled to the memory device. There is no indication in Schumann et al., Pashley et al., or Akaogi et al. of writing first data received from a first processor to a first one of a plurality of addressable banks and simultaneously reading two or more second data from a second one of the plurality of addressable banks and providing the two or more second data to a second processor. Therefore, neither Schumann et al., Pashley et al., nor Akaogi et al. either alone or in combination with Lee teach or suggest each and every element of claims 2 and 10, and therefore claims 2 and 10 should be allowed.

Claims 3-4 depend directly from claim 2 and thus include patentable limitations of claim 2. Claims 6, 8-9 depend directly from claim 5 and thus include patentable limitations of claim 5. Claim 11 depends directly from claim 10 and thus includes patentable limitations of claim 10. Therefore, claims 3-4, 6, 8-9 and 11 should be allowed.

Double Patenting Rejection

Claims 1-6 and 8-11 were provisionally rejected under the judicially created obviousness-type double patenting as being unpatentable over claims 1-15 and 28-38 of copending U.S.

Patent Application Serial No. 09/627,770. Applicant has included a Terminal Disclaimer herewith to address the rejection. In view of the Terminal Disclaimer, Applicant respectfully requests reconsideration and withdrawal of the rejection, and allowance of claims 1-6 and 8-11.

Added Claims

Claims 12-15 are added. Applicant contends that new claims 12-15 are supported by the specification as filed and thus do not constitute new matter. Claim 12 depends directly from claim 10 and thus include the patentable limitations of claim 10. Claims 13-15 depend directly from claim 1 and thus include the patentable limitations of claim 1. Therefore, claims 12-15 should be allowed. Applicant therefore respectfully requests admission and allowance of claims 12-15.

RESPONSE TO NON-FINAL OFFICE ACTION   **PAGE 9**
Serial No. 10/786,389   Attorney Docket No. 400.007US02
Title: SYNCHRONOUS FLASH MEMORY WITH CONCURRENT WRITE AND READ OPERATION

CONCLUSION

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2207.

Respectfully submitted,

Date: _12/7/04_

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